

# Fully-integrated control stacks for quantum computing in the NISQ era

**Cornelis Christiaan Bultink**

M. Tiggelman, J. Gloudemans, D. de Jong, Y. B. Kalyoncu, J. van Oven

Qblox BV, Elektronicaweg 10, Delft, The Netherlands. contact: [hello@qblox.com](mailto:hello@qblox.com)

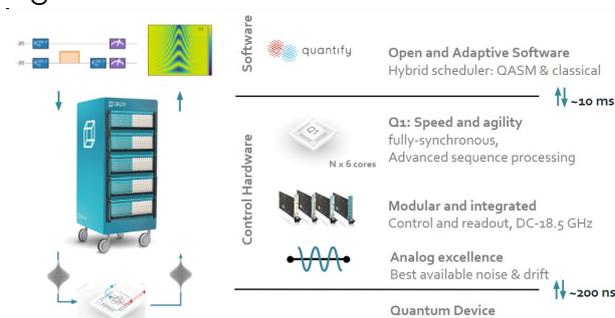
## Abstract

Reaching NISQ applications hinges on improvements in the gate fidelity and qubit number. Qblox supports this with time-efficient, ultralow-noise, and cost-effective control stacks. We introduce the Cluster system which incorporates up to 120 Q1 processors capable of sequencing pulses, their parameters, and measurement operations in real time [1]. This architecture speeds up experiments by orders of magnitude as it avoids the overhead caused by software-controlled loops. This speed-up is realized by multi-parameter real-time pulse modification and by on-board data processing (integrating, averaging, binning) of readout signals and storing up to 131072 measurement results per experimental run. The state-of-the-art signal noise level (14 nV/ $\sqrt{\text{Hz}}$  @ 1 MHz and 5 Vpp) supports improved gate fidelities and the low gain and offset drift (a few ppm/K) reduces the need for recalibrations. The Cluster supports many qubit platforms [2] with its wide frequency range from DC to 18.5 GHz while occupying less volume than 1 liter per controlled qubit. Quantify -an open-source python framework- manages the hardware stack, which allows hybrid scheduling of gate-level and pulse-level descriptions [3]. This full-stack approach opens a fast track for gate optimizations and scaling efforts towards running NISQ applications.

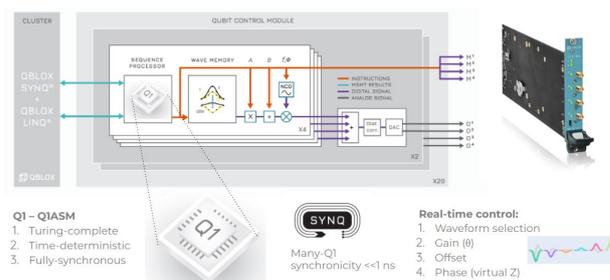
## References

- [1] W. Vlothuisen et al. (TU Delft, APS MM P48.014, 2016)
- [2] Y. B. Kalyoncu et al. (Qblox, APS MM B35.00010, 2022)
- [3] [The Quantify-Scheduler](#)

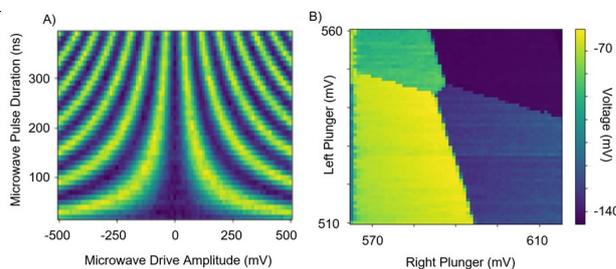
## Figures



**Figure 1:** Qblox fully-integrated control stacks provide 4 synergistic hardware and software layers for the fastest, smallest and lowest-noise control. By directly inputting and outputting pulses in the range of DC to 18.5 GHz experimental setups are simple and scalable.



**Figure 2:** The control flow in the control stack is at the heart executed by the distributed Q1 processor cores (up to 120 per Cluster). These Turing-complete and time-deterministic cores operate in full synchronicity and allow for fast and independent experiment execution with real-time parameterization of pulse properties.



**Figure 3:** Examples where order-of-magnitude speed-ups are achieved through real-time on-board compiling and on-board data analysis. A) Chevron plot for tuning the pulse amplitudes and duration of a transmon qubit, measured in 23 seconds (IMPAQT consortium) B) Charge stability diagram for tuning a Si double-dot sample, measured in 180 ms (Qutech).